Reversible ALU quantum dot cellular automata: a new design and simulation

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Abstract

Quantum dot cellular automata (QCA) technology is a potential solution to issues with nanoscale CMOS-based digital circuit fabrication because of its small size, low power consumption, and rapid latency. The arithmetic logic unit (ALU) serves as the "brain" of a modern CPU. The assembly of a reversible ALU unit using both traditional reversible blocks and an innovative design, the BS1 Block, is described in depth in this study using quantitative circuit analysis (QCA). The suggested approach has the block do all the calculations and evaluations. You may use QCA Builder to see whether the suggested design is feasible. A 30% reduction in the quantum cost, a 27% increase in the number of cells, and a 30% improvement in efficiency are the three main areas where the suggested arrangement outperforms its predecessors, according to the modeling findings. It calls for a less substantial physical footprint.

Keywords: Designer of quantum dot cellular automatas (QCAs), reversible logic, and arithmetic logic units (ALUs).

Introduction

Overconsumption of power and energy loss are the two biggest obstacles to digital circuitry improvement in systems [1]. The introduction of irreversible circuitry using nanotechnology will lead to a dramatic increase in power consumption. Using reversible processing is one approach to lowering the bar for creating new circuits [1]. Energy is wasted due to a lack of understanding. In the absence of data deletion, there will be no power loss. With K being Boltzmann's constant, T being the operating temperature in Kelvin, and n being the number of bits, the energy loss rate per bit is approximately KTLn2 [2]. Landauer established this in 1961. The number of transistors on silicon computers rises around every 18 months, according to Moore's Law [3,]. Using bidirectional gates, Bennett shown in 1973 that energy loss in such circuits may be significantly decreased or eliminated [4]. Reversible calculations save energy and do not lose data bits. When creating circuits with reversible functionality, reversible logic gates are an absolute must. If the inputs and outputs of a reversible gate are exactly the same, then the gate is a logic gate. A great deal of the work that goes into making and designing electrical device circuits is CMOS technology. Physical constraints of CMOS technology make it very challenging to build circuits on a tiny scale. The problems with CMOS technology have led to the suggestion of many alternatives. Since it does not depend on transistors, QCA technology is among the most effective choices for fabricating nanoscale digital circuitry. Small, quick, and power-efficient circuits are now within reach, thanks to this technology. At its core, quadrilateral corner array (QCA) technology is based on the QCA cell. An electron or two are sent to each of the cellular centers. Coulombic force characteristics are the basis of the system. The process by which QCA activates and deactivates cells involves moving electrons from one cell to another. Among QCA's tools are the NOT and three input majority gates [5]. The importance of processing to the efficiency of a computer is highlighted by Sousa [6]. Nanotechnology and quantum-based computing are at the forefront of this discussion, as are a number of innovative computational models. Many reversible logic gates have been proposed and constructed for use in reversible combinational and sequence circuits in the last few years [7]. A bidirectional incremented circuit was proposed and implemented by Das et al. [8] in QCA. Additionally, they created a new reversible half-adder circuit by using the Peres reversible gate. A new construction based on Feynman and Toffoli gates was proposed by Das et al. [9] to construct an encoder circuit using QCA technology. The main component of a central

processing unit (CPU) is the arithmetic logic unit (ALU). In recent years, a plethora of experiments using reversible ALUs based on QCA have been proposed and implemented. An effective bidirectional ALU unit in QCA was developed by Sasami et al. [10] as an example. They propose RUG as the foundational element of their design. The paper proposes a reversible ALU unit that makes use of QCA technology and a BS1 Block, which is a set of forty-four reversible blocks. The recommended ALU design makes use of reversible Feynman gates, Fredkin gates, and the block. Mathematical and logical operations such as adding, increasing, subtracting, and transferring, as well as OR, AND, and XOR, are all within the capabilities of the proposed system. By using QCA technology, the proposed design may outperform previous research, particularly with regard to decreased latency and footprint. The proposed layout may be simulated using Codesigned 2.0.3 [11]. This version outperforms its predecessors in terms of quantum cost, cell count, and process count as well. Finally, the following points are brought up by this piece:

- Proposing a new reversible block that is called BS1 Block
- Design of proposed block quantum structure
- Simulate the proposed block using QCADesigner 2.0.3 tool
- Proposing a new reversible ALU
- Design of a reversible ALU unit using two gates Feynman, Fredkin and the proposed block
- Simulation of the proposed ALU using the QCADesigner 2.0.3 tool
- Calculation of evaluation parameters of the proposed structure such as number of constant inputs, number of garbage outputs, latency, quantum cost and comparison with recent research

The rest of this paper is organized as follows: The QCA cell, wire construction, reversible logic, and the implementation of reversible gates are some of the basic topics covered in Section 2 of the guide to QCA technology. In Section 3, we talk about certain texts that are pertinent. We have a look at the proposed design and the moveable block in Section 4. Section 5 details the proposed architecture's modeling and compares it to comparable research. portion 6, the last portion, presents the results.

Basic QCA technology concepts

The key concepts of Quantum Computer Architecture (QCA) are introduced here, including the QCA cell, wire structure, timing idea, reversible logic, and the Feynman and Fredkin reversible gates used in the suggested ALU circuit. Figures of worth are also described, including cell count, steady intake, trash output, filled area, and quantum cost.

QCA cells

Each QCA cell in QCA technology consists of 4 holes and 2 additional electrons; these electrons are allowed to travel between the holes. Two electrons can be placed in four holes in six distinct ways, but not all of these states are permanent due to the Coulomb Effect. Cell polarization is a stable condition that happens when electrons are situated at the farthest distance, or at perpendicular spots. These are the Plus 1 and 1 phases depicted in Fig. 1, which correspond to the logic 1 and logic 0 [8, 11, 12].

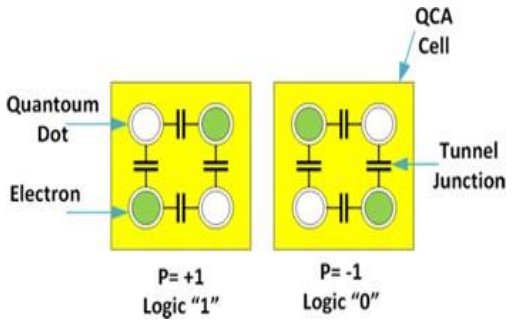


Fig. 1 Display of two stable states of the stem cell in QCA (left hand with logic 1 and right hand with logic zero) [12] .

Wire structure:

Because of the negative force of Coulomb interaction, every cell influences the cells nearby. Two neighboring cells, however, will always face each other in a way that mitigates this repulsive force. It is possible to use a matrix's QCA cells as a signal wire. Figure 2 shows two different kinds of QCA lines. Figure 2a shows that the first cell's logical number is carried to the remaining cells. Figure 2b shows a quantum wire with a cell value that is the polar opposite of the structure of the cell before it. The rooms are angled at 45 degrees. The second type, called the "complement chain," involves rotating the units 45 degrees. Cells and their corresponding pairs transmit input signals to one another. If you want a more accurate

depiction of a wire, you may stack these two models.

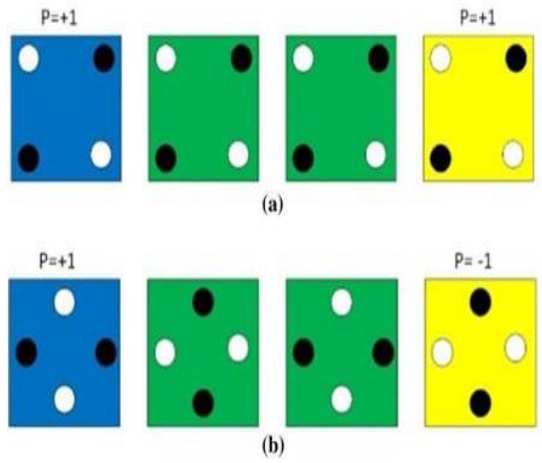
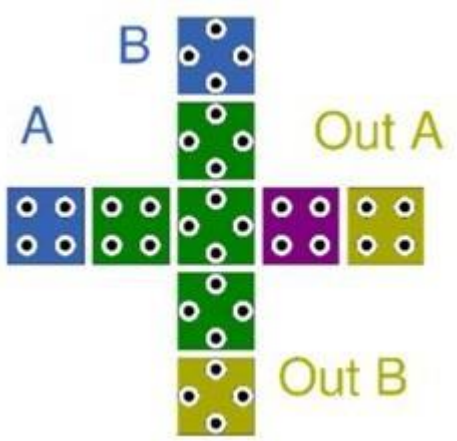


Fig. 2 a QCA standard wire; b QCA complement wire [13]

Fig. 3 Passed crossing wire model [12]



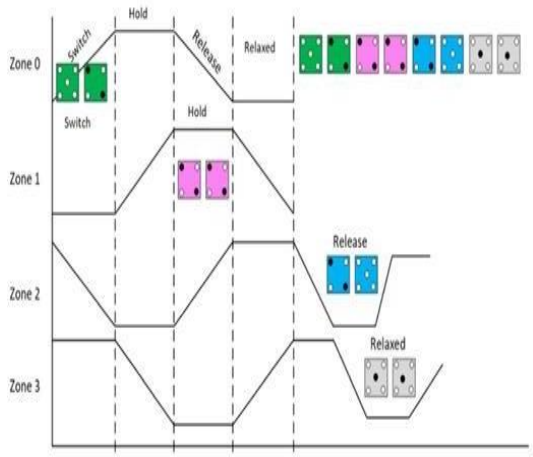


Fig. 4 Different clocking areas in QCA [17]crossing wire, which is depicted in Fig. 3. In the crossing wire model, due to the difference in cell polarity, the two wires have no effect on each other [8, 11, 12, 14, 15].

Clocking in QCA:

To improve their robustness, QCA-based circuits use clocking. A one-dimensional schedule governs each of the four steps that comprise QCA's numerical operations in their default setup. Figure 4 shows that there are four stages—Switch, Hold, Release, and Rest—that make up each QCA circuit. Each of these four steps is 90 degrees apart from the others. The energy restrictions inside the point gradually increase during this phase, and neighboring cells that are also in the switch or hold phase might impact the electrons at the points. When in the release phase, the force between the spots reduces, the electrons are no longer shielded from the electrons in nearby cells when in the hold phase.

Fig. 5 Quantum structure of Feynman gate [18]

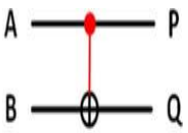
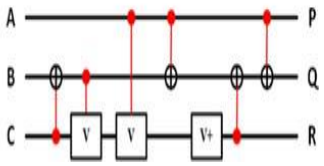


Fig. 6 Quantum structure of Fredkin gate [19]



can lessen, electrons progressively liberate, and electron movement within the cell becomes fully loose at some point [16].

Reversible logic

A bidirectional logic function is one where the output values can be used as inputs to produce the other inputs independently. It is possible to implement a bidirectional logic function with a reversible gate. The inputs and outputs of a reversible gate are both identical in quantity, and the input and output vectors are directly proportional to one another. The suggested ALU circuit's two bidirectional Feynman and Fredkin gates have their quantum structure described in Parts 2.4.1 and 2.4.2..

Feynman gate

The Feynman gate [18] is a two-input, two-output bidirectional logic gate. In Fig. 5 we see the quantum structure of this gate. P = A, Q =

AB describes the Feynman gate, which takes in two inputs (A and B) and produces two outputs (P and Q). This gate has a one for its quantum cost. This gate is used to generate spread out or eliminate the restriction that arises when designing bidirectional circuits, wherein an output can only be used to one of the other inputs of the circuit gates. It is also possible to use this gate to make an input that is a counterpart of another.

Fredkin gate

The bidirectional Fredkin gate takes in and sends out three signals. The quantum cost of this obstruction is Figure 6 shows the quantum representation of this barrier. There are three inputs (labelled A, B, and C) and three outputs (labelled P, Q, and R) on this particular Fredkin gate. These findings can be explained by the equations P = A, Q = ABAC, and R = ACAB. This gate can switch the sequence of inputs B and C as a 2 to 1 multiplexer, based on the value of input A. This structure holds if (A=0), (Q=B), (R=C), and (A=1), (Q=C), and (R=B) [19].

Figures of merit

Figures of merit are quantifiable metrics used to compare the effectiveness of one approach to others. Most scholars in the field of based reversible logic systems use criteria to gauge the efficacy of their suggested technique. This essay considers the following factors:

- Constant inputs: Inputs that need to be placed in a reversible circuit with a constant zero or one.
- Garbage output: Outputs that in the reversible circuit are not considered as the main circuit output.
- Occupied area: The required space to design and simulate a circuit based on QCA technology.
- Number of cells: The number of QCA cells used to simulate a reversible circuit.
- Quantum cost: The quantum cost of each circuit depends on the 1×1 and 2×2 reversible base gates required to design it.

Related works

Using the HNG bidirectional gate, a device was suggested by Chandra et al. [20] that can execute seven logical operations and eight numerical operations [21]. There have been several architectural adjustments, such as those to the quantum cost, latency, number of bidirectional gates, number of garbage outputs, number of continuous inputs, and so on. A three-layer ALU design with four adder gates that have been validated extensively was suggested by Goswami et al. [22]. It has 1069 individual cells, occupies 2.34 square meters, and has a lag time of two hours. This design's main drawback is the high area need. A complete adder, AND, OR, and XOR operations, as well as a QCA-based single-bit ALU, were suggested by Qadim et al. [23]. The 3 layer, 0.78 square meter structure had 464 cells and had a latency duration of 3 seconds. It will be a long-term construction project. In their proposal for a reversible ALU design, Alizadeh et al. [24] included the novel reversible gate NHG. They used a more sophisticated approach than others, but it reduced the resources needed to create a wall of the same kind. With a 4-cycle delay and 670 cells, the design occupies 0.921 m2. Using a constant input and two waste products as outputs, the system is capable of performing sixteen arithmetic and logical operations. Using a reversible multiplexer, Sen et al. [25] developed a testable reversible ALU unit. In an ALU, the reversible logic unit (RLU) and the reversible arithmetic unit (RAU) are separate components. Although these parts are shown independently, the QCA design of the proposed ALU unit is not. With nine constant inputs and fifteen variable outputs, this scheme makes use of rotating cells on a single layer. Seventeen separate mathematical and reasoning processes are within this design's capabilities. A single-bit ALU constructed from four Fredkin gates and two Toffoli gates was introduced by Chavez et al. [26] in the QCA. A four-way trash can junction makes the notion a reality. On this platform, there are a total of six viable rational procedures. An ALU was constructed by Sokoori et al. [27] using the Double Feynman gate, also known as the AND gate, a bidirectional gate.The outputs of the complete adder and the OR are chosen by the multiplexer. Using QCA technology and reversible Fredkin and HNG gates, Norouzi et al. [28] presented a reversible ALU unit. The design specifies the use of three Fredkin Gates in addition to one HNG Gate. The suggested arrangement maintains a consistent location for trash can emptying. The device can execute twenty distinct mathematical and reasoning procedures. A total of 480 parts and 0.75 square meters of surface area were used to model this arrangement.

Proposed reversible ALU.

Always essential to the proper functioning of the computer, the ALU is the brains of any digital central processing unit. Because of the risk of data loss, ALUs built using irreversible logic use a lot of power. An essential need for such designs is the prevention of such power loss. Designing the ALU unit in both directions may improve its power economy. Here we'll examine the suggested design in further detail, including the reversible BS1 Block, the reversible ALU, the table of arithmetic and logic operations that the design can accomplish, block emulation, and the design itself.

Proposed reversible BS1 Block

The proposed bidirectional BS1 Block consists of four parameters: W, X, Y, and Z for inputs and P, Q, R, and S for outputs. The following formulae may be used to simulate the results: P=M(X, Z) W, Q=Y, R=X Y Z, and S=Z. Figure 7 shows the proposed building component's quantum structure. In addition to basic arithmetic operations, this unit is capable of performing logical operations such as AND, OR, XOR, and NAND. If input W is zero, this block acts as a full adder; in this case, the carry number is produced at output P, and the result at output R is the sum of the three input values X, Y, and Z. A staggering six is the quantum cost for this area. The following are some of the main advantages that this construction element provides.Most logical procedures are constructed inThere is a single XOR gate and one set of three inputs in the logic arrangement. When used alone, it performs the duties of a bidirectional full adder.

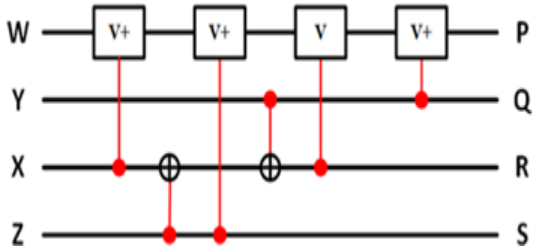


Fig. 7 The quantum structure of the proposed reversible BS1 Block

- It needs only 0.75 clock cycle to perform the operations.
- It produces only two garbage outputs.
- Its quantum cost is 6.
- Simplicity of simulating and implementing the proposed reversible block in comparison to exiting 4*4 blocks.
- Reduce the number of cells in the proposed reversible block in comparison to exiting 4*4 blocks.
- Reduce the occupied area of the proposed reversible block in comparison to exiting 4*4 blocks.
- Due to the simple logical structure and performing many computational and logical operations, this block can be used in multi-bit arithmetic and logic unit, which will be optimal compared to existing designs in terms of cell number, occupied area, latency and quantum cost.

Proposed reversible ALU scheme.

A new BS1 Block, reversible Feynman gates and Fredkin gates are also part of the plan. Figure 8 depicts the quantum form of the ALU unit that has been suggested. The suggested layout calls for C2 and C3 to regulate the Feynman gates' A and B inputs, respectively. Logic gates that may operate on either A or B, or their counterparts, are called Feynman bidirectional gates. Put the desired gate's control input to zero if you need input A or B, and to one if you require the matching input of input B. As an example, the suggested construction block receives Q from the second Feynman gate when C2 = 0 and An when C2 = 1. The suggested architecture utilizes the Fredkin gate to choose between two outputs, O1 and O2. In the suggested configuration, C1 is connected to the control input of the Fredkin gate. With C1= 0, the Fredkin results are the same.

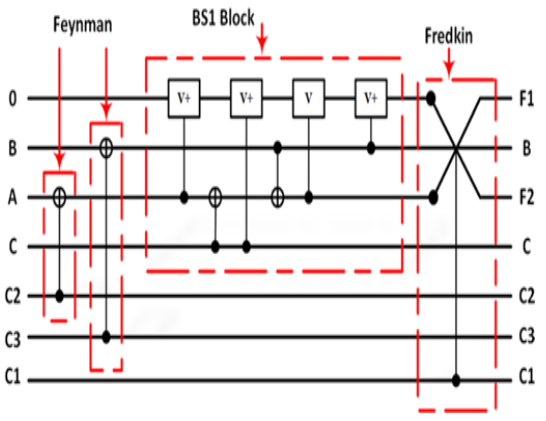


Fig. 8 Quantum structure of the proposed reversible ALU unit

If C1 = 1, the results are flipped from Q = B and R = C to Q = C and R = B. As an added bonus, the suggested BS1 Block can perform both logical and numeric calculations. This plan has a quantum cost of thirteen.

Logic and arithmetic operations of the proposed ALU unit

This system offers twenty different mathematical and logical functions. In the proposed design, there are two outputs denoted as F1 and F2 and six inputs denoted as C1, C2, C3, A, B, and C. Two outputs, B and C, may be used as inputs in the subsequent block; the data stream entering this structure is reliable and generates zero garbage. Among the many mathematical and logical operations that this structure is capable of performing are AND, NOR, XOR, NAND, XNOR, OR, transfer, input reversal, increase, borrowing (subtracting with borrowed number), and carrying. You can see all the possible mathematical and logical operations that the proposed system can do in Table 1.

Simulation and comparison of results

To model the suggested architecture, this article makes use of the Codesigned 2.0.3 application. Quickly create, arrange, and simulate QCA circuits with the help of Codesigned software [5]. Simulation and performance findings for the proposed BS1 Block, the proposed ALU circuit, and a contrast and assessment of the proposed design in light of prior study are discussed below. Except for the amount of samples, which is set to 128,000 by default, all other modelling settings have present values.

Table 1 Proposed ALU logic and arithmetic operations

Control Inputs			Operands			Outputs		
C_1	C_2	C_3	A	B	C	F_1	F_2	
0	0	0	A	0	0	0	A	
0	0	0	A	1	0	A	$\bar{A}$	
0	0	0	A	0	1	C_{out}	$A+1$	
0	0	0	A	B	C_i	C_{out}	$A+B$	
0	1	0	A	B	C_i	Brw	$A-B$	Arithmetic Operations
0	1	1	A	B	1	Brw	B − A	
0	1	0	A	B	0	$\bar{A}B$	$\bar{A}\oplus B$	
0	1	1	A	B	0	$\bar{A}\,\bar{B}$	$\bar{A}\oplus\bar{B}$	
1	0	0	A	B	0	$A\oplus B$	AB	
1	0	0	A	B	1	$A\odot B$	$A+B$	
1	0	1	A	B	0	$A\oplus\bar{B}$	$A\,\bar{B}$	
1	0	1	A	B	1	$A\oplus B$	$A+\bar{B}$	Logic Operations
1	1	0	A	B	0	$\bar{A}\oplus B$	$\bar{A}B$	
1	1	0	A	B	1	$\bar{A}\oplus\bar{B}$	$\bar{A}+B$	
1	1	1	A	B	0	$\bar{A}\oplus\bar{B}$	$\bar{A}+\bar{B}$	
1	1	1	A	B	1	$A\odot B$	$\bar{A}\bar{B}$	

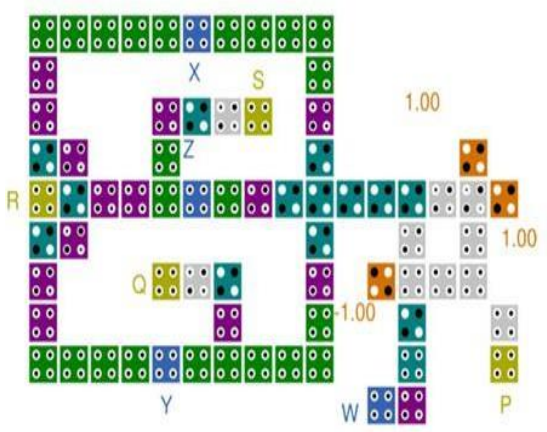


Fig. 9 BS1 Block simulation by QCA cells

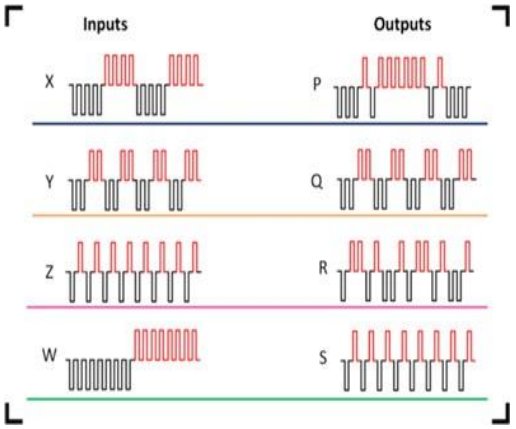


Fig. 10 the simulation result of BS1 Block

Proposed reversible block simulation BS1 block.

In Fig. 9, we can see the results of the suggested QCA-based modelling of the BS1 Block. Inputs (W, X, Y, and Z) lead to products (P, Q, R, and S). This section constitutes the bulk of the planned ALU. The suggested BS1 Block wasmodelled with the help of two XOR gates and a consensus user. 72 cells with diameters of 18 nanometre, area of 0.08 m2, and a delay of 3 stages' clock cycles were used to model the block. Similarly, Fig. 10 displays the simulation's outcome. It can be seen from Fig. 10 that the values P = 1, Q = 1, R = 0, and S = 1 result from the inputs W = 0, X = 0, Y = 1, and Z = 1. The values P, Q, R, and S are produced when the inputs W, X, Y, and Z are all 1.

Proposed reversible ALU simulation.

Figure 11 shows the results of a test of the suggested QCA-based bidirectional ALU. The architecture consists of a Fredkin gate, two Feynman gates, and the suggested bidirectional BS1 Block for conducting logic and math functions. The suggested ALU relies heavily on the BS1 Code. The BS1 Block takes in signals at A, B, C, and S. In the suggested design, S equals zero, A, B, and C are set from the outputs of the two Feynman gates, and D is a constant. All of these numbers are taken from Table 1. The P and R outputs of BS1 Block serve as Fredkin inputs, which are used as multiplexers in the ALU architecture to define the necessary processes and decide the end output. The suggested ALU exercise is based on QCA and is carried out on a 0.52 m2 region with 350 cells operating in 3 different clock pulse zones. Figure 12 depicts the outcome of a modelling of the circuit.

Evaluation and comparison

The suggested ALU is compared to other works in this field in terms of metrics like number of processes, delay, quantum cost, number of cells, and area taken up. The ALUs suggested in [24, 28] will be evaluated in QCA-based experiments in terms of cell density and surface area occupancy to determine which is superior. When compared to planned ALUs, the suggested ALU has many more cells, making it more efficient. When compared to these ALUs, it also performs better in terms of delay and space utilization. Table 2 provides an overview of the differences made between the provided ALUs and the ALUs generated using QCA. Compared to [24, 28], Fig. 13 displays the suggested method's increase in percentage form. When compared to the approaches in [24] and [28], the suggested ALU improves the filled area measure by 45% and 30%, respectively.

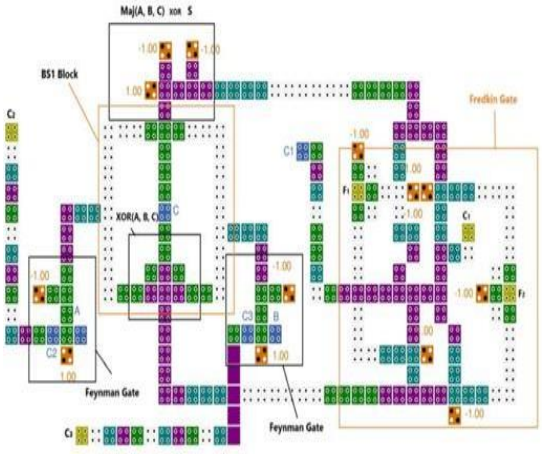
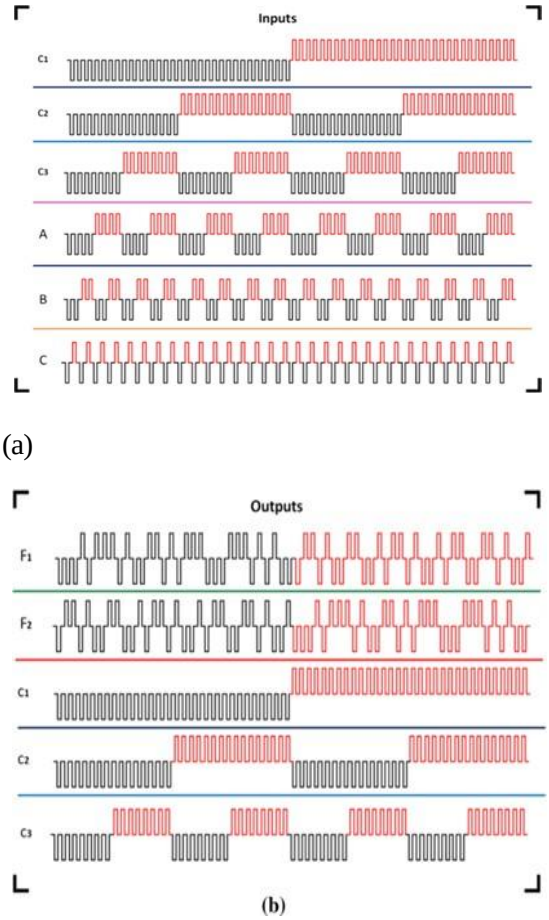


Fig. 11 Simulation of an ALU unit designed using QCA cells



(a)

(b)

Fig. 12 Simulation result; a inputs and b outputs

Conclusion and future work:

In this work, we introduce a reversible ALU that consists of a four-by-four reversible block (the BS1 Block), a three-by-three reversible Fredkin gate, and two two-by-two Feynman

gates. The suggested BS1 Block is a reversible 44 block with a quantum cost of 6.

Table 2 Comparison of ALU presented with previous researches.

Ref.	Operations	Quantum cost	Latency	Number of cells	Area (μm^2)
[24]	16	21	16	670	0.921
[23]	4	14	16	464	0.78
[22]	21	18	12	1069	2.34
[27]	4	13	12	332	0.38
[28]	20	20	15	480	0.75
Proposed	20	13	12	350	0.52

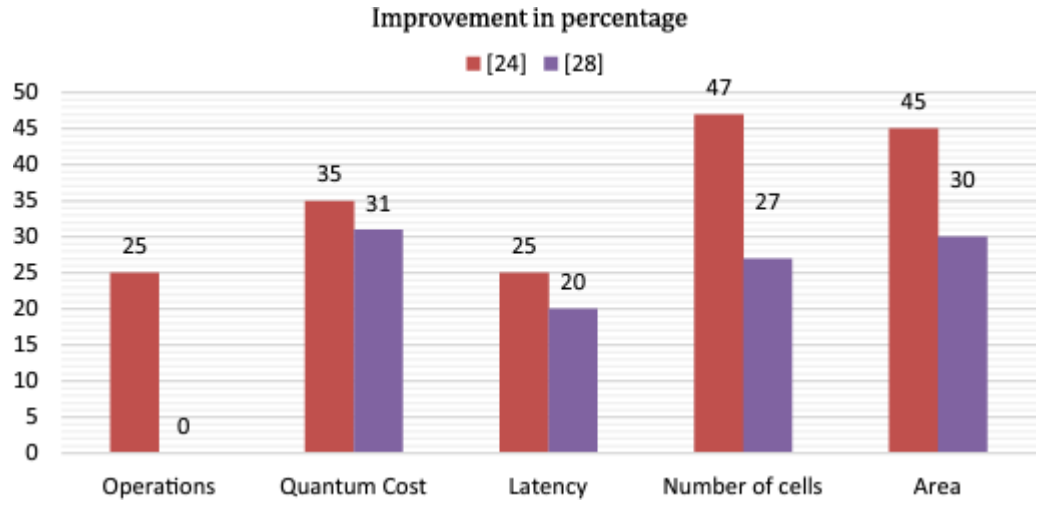


Fig. 13 Improvement in percentage of the proposed method compared to previous studies.

Built into the architecture of the BS1 Block are two XOR gates and one three-input consensus. A bidirectional ALU has several potential advantages, such as a smaller footprint, less latency, fewer cells, and lower quantum cost. The proposed concepts are tested using the Codesigned 2.0.3 software. To model the proposed bidirectional ALU, QCA technology is used. There are 250 units in the proposed arrangement, which takes up 0.30 m2. Our QCA-designed bidirectional ALU surpasses the current state-of-the-art in evaluation criteria such as cell count, latency, and filled area. Future work on innovative logical reversible gates, like as XOR, might cut down on cell count, quantum cost, process count, and latency.

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